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"Survey on Carry Look Ahead Adder"

***Poornima Shrivastava*[*], *Prof. Balram Yadav*[**] *and Prof Bharti Chourasia*[**]**

[*]*M. TECH Student (VLSI), Scope College of Engineering, Bhopal, (MP), INDIA*

[**]*Department of Electonics & Communication Engineering,*
Scope College of Engineering, Bhopal, (MP), INDIA

(Corresponding author: Poornima Shrivastava)
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ABSTRACT: A carry-look ahead adder improves speed by reducing the amount of time required to determine carry bits. It can be contrasted with the simpler, but usually slower, ripple carry adder for which the carry bit is calculated alongside the sum bit, and each bit must wait until the previous carry has been calculated to begin calculating its own result and carry bits . The carry-look ahead adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bits.

Keywords: Adder, CLA, RCA, CMOS.

I. INTRODUCTION

THE ADDERS: Addition is the most common and often used arithmetic operation on microprocessor, digital signal processor, especially digital computers. Also, it serves as a building block for synthesis all other arithmetic operations. Therefore, regarding the efficient implementation of an arithmetic unit, the binary adder structures become a very critical hardware unit. In any book on computer arithmetic, someone looks that there exists a large number of different circuit architectures with different performance characteristics and widely used in the practice. Although many researches dealing with the binary adder structures have been done, the studies based on their comparative performance analysis are only a few. In this project, qualitative evaluations of the classified binary adder architectures are given. Among the huge member of the adders we wrote VHDL (Hardware Description Language) code for Ripple-carry, Carry-select and Carry-look ahead to emphasize the common performance properties belong to their classes. In the following section, we give a brief description of the studied adder architectures. With respect to asymptotic delay time and area complexity, the binary adder architectures can be categorized into four primary classes.. The given results in the table are the highest exponent term of the exact formulas, very complex for the high bit lengths of the operands. The first class consists of the very slow ripple-carry adder with the smallest area. In the second class, the carry-skip, carry-select adders with multiple levels have small area requirements and shortened computation times. From the third class, the carry-look ahead adder and from the fourth class, the parallel prefix adder represents the fastest addition schemes with the largest area complexities. Here the study of different aspect of Carry Look Ahead Adder is being presented. The proposed adder combines the advantage of both the static and dynamic designs, which exhibits lower leakage, higher noise immunity and high speed. Reversible logic can be applied in fields such as low power CMOS circuits, quantum computation and DNA computing. Carry Look-ahead Adder (CLA) is a kind of optimization to conventional RCA, which overcomes the defects of RCA such as low computing efficiency and long delay, so CLA becomes one type of wide-used adders. In this paper, we present a survey on 16-bit CLA which shows enhance the computing efficiency of adder and decline the amount of energy dissipation based on reversible logic theory. In this paper we present a high performance and power efficient CLA implementation.

The circuit density and the energy-efficiency of the CMOS integrated circuits have been dramatically increased by scaling down their physical sizes using the cutting-edge circuit fabrication processes. However, the limit on improving their energy-efficiency is approaching; the power consumption caused by the leak currents and the long inter connect resistances cannot be ignored and occupies the large amount of the total power consumption in the recent sub-100 nm CMOS devices. Other methods, such as multi core processors and general-purpose computing on graphics processing units (GPGPU), are now introduced in order to improve the energy-efficiency, but they could result in merely limited extending of the growth of the CMOS technologies.

The main idea behind the CLA adder is an attempt to generate all incoming carries in parallel; therefore, it increases the performance.

Carry Look Ahead Adders (CLA): The key to speeding up addition is determining the carry in to the high-order bits sooner. There are a variety of schemes to anticipate the carry so that the worst case scenario is a function of the log2 of the number of bits in the adder. These anticipatory signals are faster because they go through fewer gates in sequence, but it takes many more gates to anticipate the proper carry A key to understanding fast-carry schemes is to remember that, unlike soft ware, hardware executes in parallel whenever inputs change.

Fast Carry Using "Infinite" Hardware

As we mentioned earlier, any equation can be represented in two levels of logic. Since the only external inputs are the two operands and the Carry In to the least significant bit of the adder, in theory we could calculate the Carry In values to all the remaining bits of the adder in just two levels of logic.

For example, the Carry In for bit 2 of the adder is exactly the Carry Out of bit 1, so the formula is:-

CarryIn2 = (b1 . CarryIn1) + (a1 . CarryIn1) + (a1 . b1)

Similarly, CarryIn1 is defined as:-

CarryIn1 = (b0 . CarryIn0) + (a0 . CarryIn0) + (a0 . b0)

We can imagine how the equation expands as we get to higher bits in the adder; it grows rapidly with the number of bits. This complexity is reflected in the cost of the hardware for fast carry, making this simple scheme prohibitively expensive for wide adders.

Ripple carry adder

A ripple carry adder is a digital circuit that produces the arithmetic sum of two binary numbers. It can be constructed with full adders connected in cascaded with the carry output from each full adder connected to the carry input of the next full adder in the chain the interconnection of four full adder (FA) circuits to provide a 4-bit ripple carry adder. Notice from that the input is from the right side because the first cell traditionally represents the least significant bit (LSB). Bits and in the figure represent the least significant bits of the numbers to be added. The sum output is represented by the bits

Ripple carry adder delays

In the ripple carry adder, the output is known after the carry generated by the previous stage is produced. Thus, the sum of the most significant bit is only available after the carry signal has rippled through the adder from the least significant stage to the most significant stage. As a result, the final sum and carry bits will be valid after a considerable delay. Table shows the delays for several CMOS gates assuming all gates are equally loaded for simplicity.

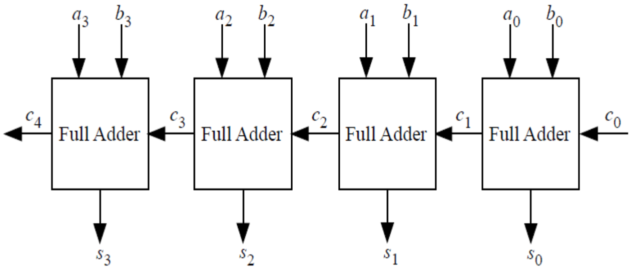
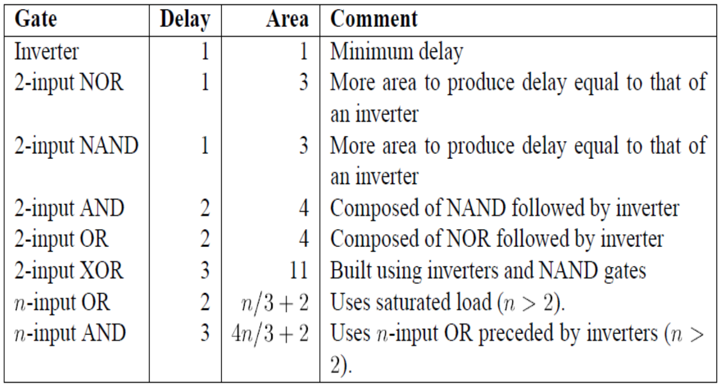


Fig. 1. 4-bit full adder.

Table 1: CMOS gate delays and areas normalized relative to an inverter.



Gate	Delay	Area	Comment
Inverter	1	1	Minimum delay
2-input NOR	1	3	More area to produce delay equal to that of an inverter
2-input NAND	1	3	More area to produce delay equal to that of an inverter
2-input AND	2	4	Composed of NAND followed by inverter
2-input OR	2	4	Composed of NOR followed by inverter
2-input XOR	3	11	Built using inverters and NAND gates
n-input OR	2	$n/3+2$	Uses saturated load ($n > 2$).
n-input AND	3	$4n/3+2$	Uses n-input OR preceded by inverters ($n > 2$).

All delays are normalized relative to the delay of a simple inverter. The table also shows the corresponding gate areas normalized to a simple minimum-area inverter. Note from the table that multiple-input gates have to use a different circuit technique compared to simple 2-input gates.

Fast Carry Using the First Level of Abstraction: Propagate and Generate

Most fast-carry schemes limit the complexity of the equations to simplify the hardware, while still making substantial speed improvements over ripple carry. A carry-look ahead adder relies on levels of abstraction in its implementation.

Let’s factor our original equation as a first step:

$ci + 1 = (bi . ci) + (ai . ci) + (ai . bi)$

$= (ai . bi) + (ai + bi) . ci$

Fast Carry Using the Second Level of Abstraction

First, we consider this 4-bit adder with its carry-look ahead logic as a single building block. If we connect them in ripple carry fashion to form a 16-bit adder, the add will be faster than the original with a little more hardware.

To go faster, we’ll need carry look ahead at a higher level. To perform carry look ahead for 4-bit adders, we need to propagate and generate signals at this higher level. Here they are for the four 4-bit adder blocks:-

$P0 = p3 . p2 . p1 . p0$

$P1 = p7 . p6 . p5 . p4$

$P2 = p11 . p10 . p9 . p8$

$P3 = p15 . p14 . p13 . p12$

Carry look ahead offers a faster path than waiting for the carries to ripple through all 32 1-bit adders. This faster path is paved by two signals, generate and propagate. The former creates a carry regardless of the carry input, and the latter passes a carry along.

II. LITERATURE SURVEY ON LOOK AHEAD CARRY GENERATOR

The fundamental operation in any digital system. The propagation time is more in addition due to large time required for the carry bits.A carry look ahead adder improves the speed by reducing the time required [13] to solve carry bits. It is mostly used in electronics devices. An efficient implementation of two bit carry look ahead adder is proposed using fully automatic and semi-custom design steps. This paper is a comparison of complexity of automatic generated design against semi-custom design. A two bit CLA adder was Designed in 90nm low power high speed technology. The performance of the CLA is measured.

VLSI technology is used where we can design complex system like Analog or Digital circuit on single chip[1]. In devices for example Laptops, cell phones power consumption become major concern in designing. Due to limited power the circuitry involved must be designed such that they consume less power because large power consumption requires expensive cooling circuitry [2]. The major issue of concern is heat dissipation and power consumption in any circuit [3]. Addition is the widely used arithmetic operation and also time consuming. Addition is the speed limiting factor to processors. As far as we are concern with high performance and speed of the process we have to increase the speed of the addition [4]. Adders are very significant components in digital systems because they are widely used in basic digital operations for example Subtraction, Multiplication and Division, hence increasing the performance of adder would advance the execution of binary operation inside a circuit[5]. High speed adders include the Carry look Ahead Adder, Carry select Adder, Carry Skip Adder and combination of these. In high speed adders the basic principle of CLA adder is dominant, only the delay of carry can be improved[6].Carry look ahead adder’s speed is usually determined by the lowest carry path delay. Its path is data dependent. Basic carry look ahead principle was developed by Weinberger and Smith [7]. In this paper, I represent two approaches one is fully automatic approach and the other is Semi-custom approach [8]. generated per bit position shows that these signals are generated in parallel. It is apparent that each carry bit is generated independent of the previous carry and the sum bit depends on the value of the previous carry bit. In look ahead carry adder, carry is generated in parallel by using look ahead carry circuit. Look ahead carry circuit contains two level AND-OR circuit.

The CLA adder using two 1-bit full adders. The output of full adder is carry propagate, carry generate and the sum of respective bits. The carry propagate and carry generate bits are given to the carry look ahead adder and the final carry is generated by CLA generator. The basic logic gates used in this CLA adder is Exclusive OR gate, AND gate and OR gate. The fig 2 shows CLA adder using logic gates. Ain and the bin are the bits to be added and cin is taken as any previous carry input

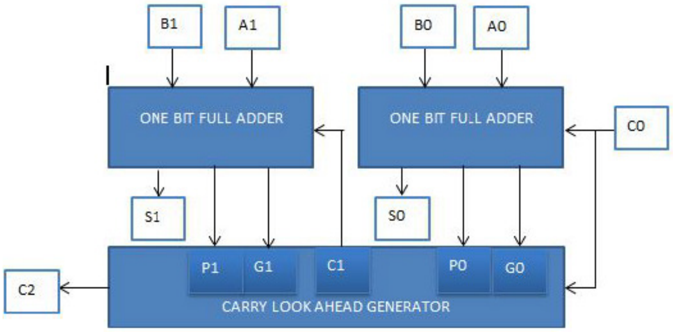


Fig. 2. CLA using Full adder.

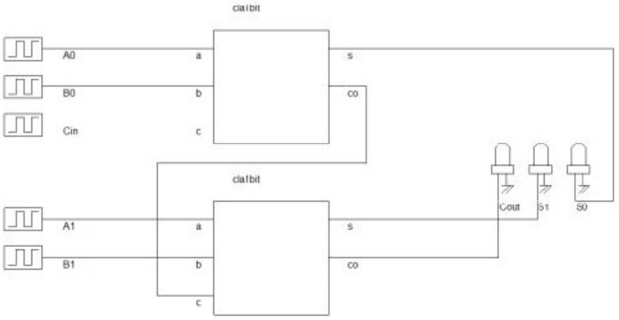


Fig. 3. Block diagram of CLA adder.

This paper gives the survey on look-ahead carry generators. Here some papers are discussed below. Nirmal have designed a high speed 256-bit carry look ahead adder using 22nm strained silicon technology. The proposed adder combines the advantage of both the static and dynamic designs, which exhibits lower leakage, higher noise immunity and high speed. The speed performance of the proposed 256-bit adder is significantly improved by computing the even and the odd carries separately by using two separate Manchester carry chains. The circuit is simulated in HSPICE in the high performance 22nm PTM strained silicon CMOS technology with a supply voltage of VDD 256- bit adder implemented using 8-bit adder modules shows significant operating speed improvement compared to the conventional 256-bit adder based on the standard 4-bit MCC adder modules.

Demonstrates the detailed design of carry look ahead adder with the single electron tunneling based threshold logic. Tunneling is a mechanism in which a single electron can cross a sandwiched structure of insulating layer between two conducting materials known as tunnel junction.

The proposed circuit is simulated in SIMON environment. The simulated input and output waveform confirm the proper functioning of the designed circuit. The stability plots of the proposed are also discussed In this paper they have a 16 bit carry look-ahead adder is constructed by four 4 digits groups based on the theory of reversible logic, which has the advantages of theoretical zero power dissipation and high efficiency. This 16-bit Carry Look-ahead Adder designed by reversible logic has advantages of short delay and low power dissipation, so it can be applied to quantum computing, wireless sensors and other areas require very low power dissipation very well. In this paper they have carry look ahead adder using using Dual Mode Logic (DML) topologies. DML logic switches between the static and dynamic mode of operations. In dynamic mode achieves higher performance with increase in power consumption and in static mode, DML logic achieves low power dissipation albeit with reduced performance.

This feature allowed implementing CLA by selection of carry path based on input vectors. A 4-bit CLA was designed in 45nm TSMC technology using Cadence Virtuoso Design. Simulation results showed gain in speed albeit with increase in power and area when compared to the conventional CMOS logic. In this paper they have presented a high performance and power efficient CLA implementation

In this paper they have designed an 8-bit carry look-ahead adder (CLA) using an AQFP cell library based on the AIST Nb 2.5 kA/cm2 standard process (STP2) and evaluated its circuit properties. The CLA is composed of 1224 critically-dumped 50-µA Josephson junctions, which occupy the area of 1.74 × 0.99 mm2 . Simulation results show that the CLA has a wide bias margin of ±29.5%, and the energy dissipation is 16.4 aJ per clock cycle at 5-GHz operation.designed SOA-SMZI-based 2-bit CLA. This scheme can easily and successfully be extended and implemented for any higher number of input digits e.g., 4-bits, 16 bits, 32 bits etc. by proper incorporation of optical switches recursivel arithmetic logic unit, and its design compared to previous work in programmable ALU design. The novel 1-bit ALU required only minimal increase in quantum cost and delay due to the MG design, which also allowed for increased functionality for the programmer. Next, we presented reversible implementations of ripple carry adder, reversible carry-select adder and reversible carry look-ahead adder. A reversible implementation of the carry logic presented in the Kogge-Stone was presented and verified.a low-cost fault-tolerant Carry Look-Ahead (CLA) adder which consumes much less power and area overheads in comparison with other fault-tolerant CLA adders. Analytical this adder corrects all single-bit and multiple-bit transient faults. The Power-Delay Product (PDP) and area overheads of this technique are decreased at least 82% and 71%, respectively, as compared to adders which use traditional TMR, parity prediction, and duplication techniques.

A low-power, Asynchrobatic (asynchronous, quasiadiabatic), sixteen-bit, radix-four, parallel-prefix adder circuit is presented (David *et al*.,). The results show that it is an efficient, low power design, and that as would be expected with an asynchronous design, its performance is determined by its operating conditions. On a 0.35µm CMOS process, under “typical” process conditions, operating at an effective frequency of 22MHz, an addition can be performed using 69pW, with 48.3pW used by the control logic and 20.7pW by the data-path. The adder style chosen for this demonstration was the parallel prefix structure . However, because of the nature of the Asynchrobatic pipeline, it was decided to use a radixfourn structure rather than the more common radix-two structure, as this reduces the number of stages in the Asynchrobatic pipeline, thus making the design more efficient.

CONCLUSION

Various designs proposed for the implementation of CLA includes strained silicon technology, single electron tunneling based threshold logic, reversible logic, DML logic using TSMC technology, SOA-SMZI based design, asynchronous quasi static adiabatic design etc . Based on the above design process implementation using 2 bit,4 bit,8 bit,16 bit,32 bit,256 bit CLA has been done. Depending upon the requirement different techniques used are of prime importance each, but the use of 256 bit CLA using strained silicon technology seems more effective as it has the advantage of being low in leakage, high speed as well as it has noise immunity, though the overall cost being more. When stability is of prime importance single electron tunneling based threshold logic seems more effective. The implementation of 16 bit CLA using reversible logic is not very fruitful as it seems more efficient theoretically, though it has the advantage of being short delay over other techniques used. DML logic is not very effective as it works on dual mode where in one mode it has more power consumption ,as our interest is in low power consumption. Implementation of 2 bit CLA using SOA-SMZI ,is helpful in the case where same can be extended to higher bit CLA. As per cost point of view fault tolerant CLA is better having the advantage of correcting single and multiple bit transient faults. As far as operating conditions is concerned Asynchronous quasi static adiabatic design is favorable.

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